



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|------------------------------------------------------------------------------|-------------|----------------------|---------------------|------------------|
| 10/700,177 | 11/03/2003 | Mukesh K. Puri | 03-0291 | 3593 |
| 24319 | 7590 | 03/21/2007 | EXAMINER | |
| LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 MILPITAS, CA 95035 | | | KERVEROS, JAMES C | |
| ART UNIT | | PAPER NUMBER | | |
| 2138 | | | | |
| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE | | |
| 3 MONTHS | 03/21/2007 | PAPER | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| | | |
|------------------------------|-------------------|--------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 10/700,177 | PURI ET AL. |
| | Examiner | Art Unit |
| | JAMES C. KERVEROS | 2138 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 November 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-18 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 03 November 2003 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All
 - b) Some *
 - c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) Notice of Informal Patent Application
- 6) Other: _____

DETAILED ACTION

This is a non-Final Office Action in response to the present US Application filed November 3, 2003. Claims 1-18 are presently under examination and still pending in the Application.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings Fig. 1-3 are informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 12 recite the limitation, "making an on-chip assessment of amount of repair of a memory", which renders the claim indefinite, because the expression "of

amount of repair" is an abstract expression, which fails to clearly define the type or the quantity of repair required for the memory under test/repair.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Beffa et al. (US 6,477,662) issued: November 5, 2002, filed: August 31, 2000.

Regarding independent Claims 1, 12, Beffa discloses a method and apparatus for implementing repairs on a memory device, using an on-chip self-test and repair circuitry, Figs. 2, 6 and 7, comprising:

Making an on-chip repair assessment of a memory array 204 on a semiconductor chip DAM 200 using the on-chip self-test and repair circuitry by finding failures and repairing must and preferred repairs on the DRAM. When a running total of the number of failures (counter 220) for each row and column equals or exceeds a predetermined value stored in (register 221), then the row or column is determined to be a must-repair

or a preferred repair, thus flagging any memory as a fail. Rows to be repaired are substituted with redundant memory rows and columns to be prepared are substituted with redundant memory columns, see Abstract.

Regarding Claims 2, 3, Beffa discloses loading a counter (register 221) with a predetermined value, which is initially set at the number of initially available redundant rows or columns, during DRAM production or manufacturing testing, and it is gradually decremented to reflect used redundant rows and columns.

Regarding Claims 4-11, Beffa discloses repair circuitry 223, under control of circuitry 222, contains logic necessary to substitute a designated redundant row or column for a failed row or column, using process 640, shown in detail in Fig. 7, which repairs the remaining non-must-repair and non-preferred-repair cell defects that may still exist after process 635 has been completed.

Regarding Claims 13-18, Beffa discloses reliability controller (test circuitry 214) comprising logic (Control circuitry 222), a counter (220) in communication with the logic, and a register (221) set in communication with the logic. Counter 220 contains a running total of the number of failures, and when the running total of the number of failures for each row and column equals or exceeds a predetermined value stored in (register 221), then the row or column is determined to be a must-repair or a preferred repair, thus flagging any memory as a fail. Register 221 contains a predetermined value, which is initially set at the number of initially available redundant rows or columns, during DRAM production or manufacturing testing, and it is gradually decremented to reflect used redundant rows and columns.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

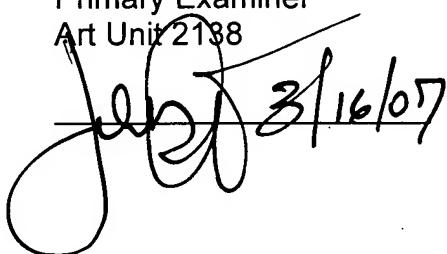
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decayd can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Date: 16 March 2007
Office Action: Non-Final Rejection

U.S. Patent and Trademark Office
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov

JAMES C KERVEROS
Primary Examiner
Art Unit 2138



3/16/07